Chapter 5: Transistor Bias Circuits

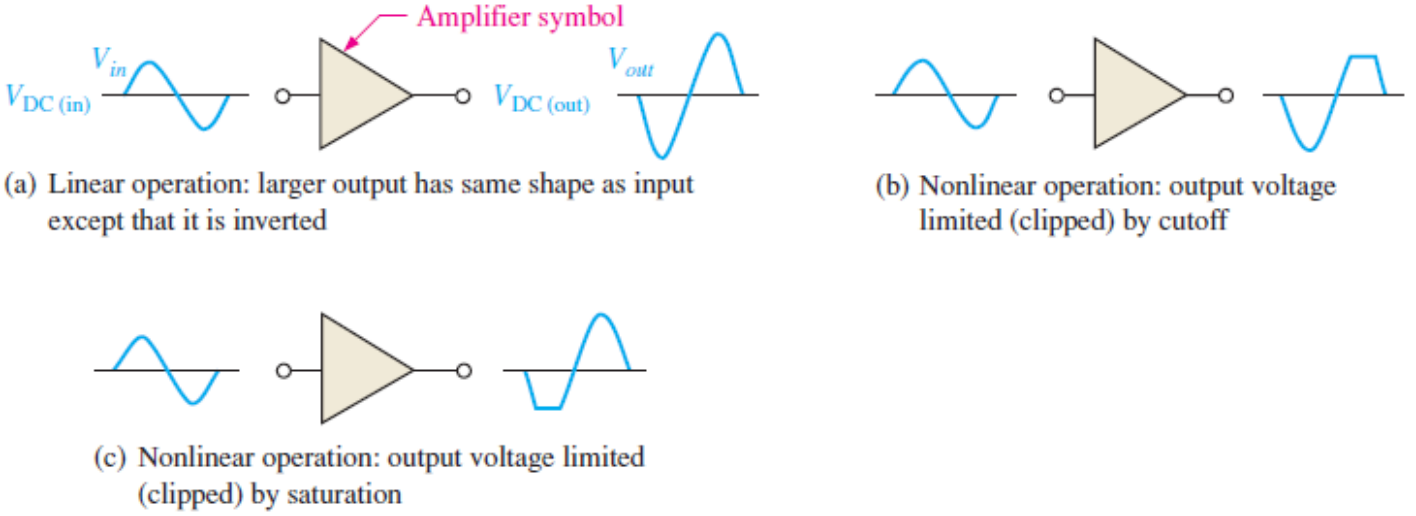
A transistor must be properly biased in order to operate as an amplifier. DC biasing is used to establish fixed dc values for the transistor currents and voltages called the *dc operating point* or *quiescent point* (*Q-point*). In this chapter, several types of bias circuits are discussed. This material lays the groundwork for the study of amplifiers, and other circuits that require proper biasing.

5.1 The DC Operating Point

A transistor must be properly biased with a dc voltage in order to operate as a linear amplifier. A dc operating point must be set so that signal variations at the input terminal are amplified and accurately reproduced at the output terminal. When we bias a transistor, we establish the dc voltage and current values. This means, for example, that at the dc operating point, I_C and V_{CE} have specified values. The dc operating point is often referred to as the Q-point (quiescent point).

DC Bias

Bias establishes the dc operating point (**Q-point**) for proper linear operation of an amplifier. If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figure 5–1 shows the effects of proper and improper dc biasing of an inverting amplifier. In part (a), the output signal is an amplified replica of the input signal except that it is inverted, which means that it is 180° out of phase with the input. The output signal swings equally above and below the dc bias level of the output, $V_{DC(out)}$. Improper biasing can cause distortion in the output signal, as illustrated in parts (b) and (c). Part (b) illustrates limiting of the positive portion of the output voltage as a result of a Q-point (dc operating point) being too close to cutoff. Part (c) shows limiting of the negative portion of the output voltage as a result of a dc operating point being too close to saturation.



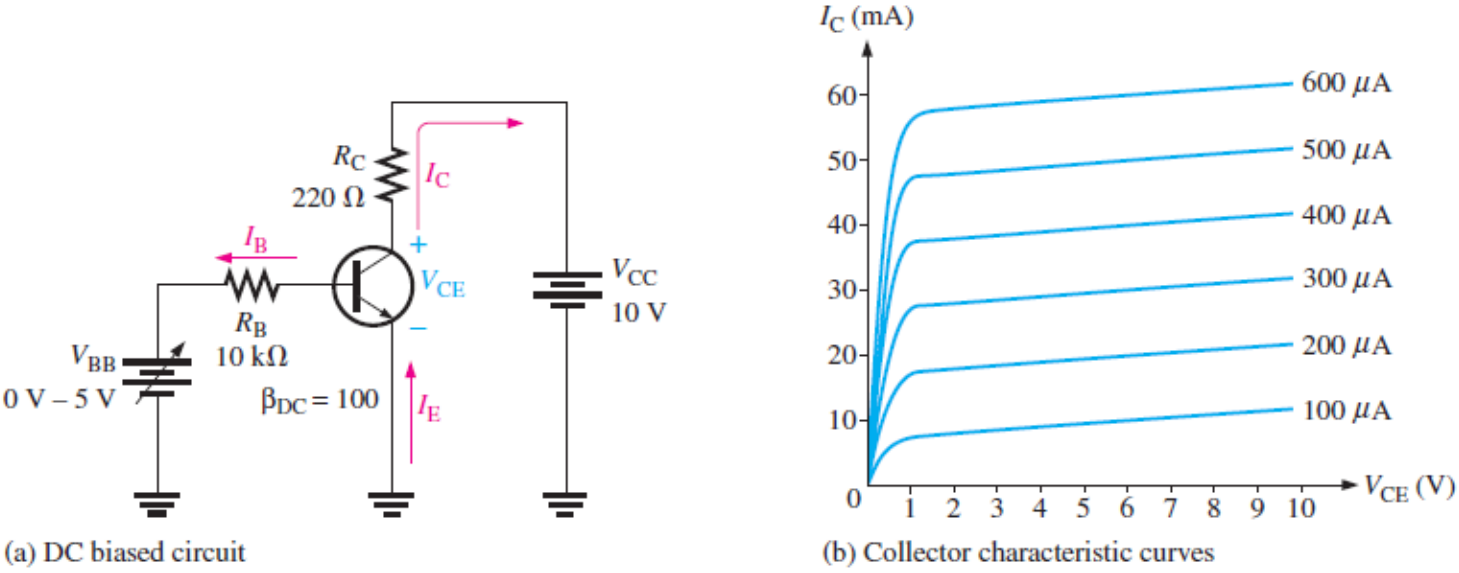
(a) Linear operation: larger output has same shape as input except that it is inverted

(b) Nonlinear operation: output voltage limited (clipped) by cutoff

(c) Nonlinear operation: output voltage limited (clipped) by saturation

FIGURE 5–1: Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol).

Graphical Analysis The transistor in Figure 5–2(a) is biased with V_{CC} and V_{BB} to obtain certain values of I_B, I_C, I_E, and V_{CE}. The collector characteristic curves for this particular transistor are shown in Figure 5–2(b); we will use these curves to graphically illustrate the effects of dc bias.



(a) DC biased circuit

(b) Collector characteristic curves

FIGURE 5–2: A dc-biased transistor circuit with variable bias voltage (V_{BB}) for generating the collector characteristic curves shown in part (b).

In Figure 5–3, we assign three values to I_B and observe what happens to I_C and V_{CE}. First, V_{BB} is adjusted to produce an I_B of 200 μA, as shown in Figure 5–3(a). Since $I_C = \beta_{DC} I_B$, the collector current is 20 mA, as indicated, and

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (20\text{ mA})(220\ \Omega) = 10\text{ V} - 4.4\text{ V} = 5.6\text{ V}$$

This Q-point is shown on the graph of Figure 5–3(a) as Q_1.

Next, as shown in Figure 5–3(b), V_{BB} is increased to produce an I_B of 300 μA and an I_C of 30 mA.

$$V_{CE} = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 10\text{ V} - 6.6\text{ V} = 3.4\text{ V}$$

The Q-point for this condition is indicated by Q_2 on the graph.

Finally, as in Figure 5–3(c), V_{BB} is increased to give an I_B of 400 μA and an I_C of 40 mA.

$$V_{CE} = 10\text{ V} - (40\text{ mA})(220\ \Omega) = 10\text{ V} - 8.8\text{ V} = 1.2\text{ V}$$

Q_3 is the corresponding Q-point on the graph.

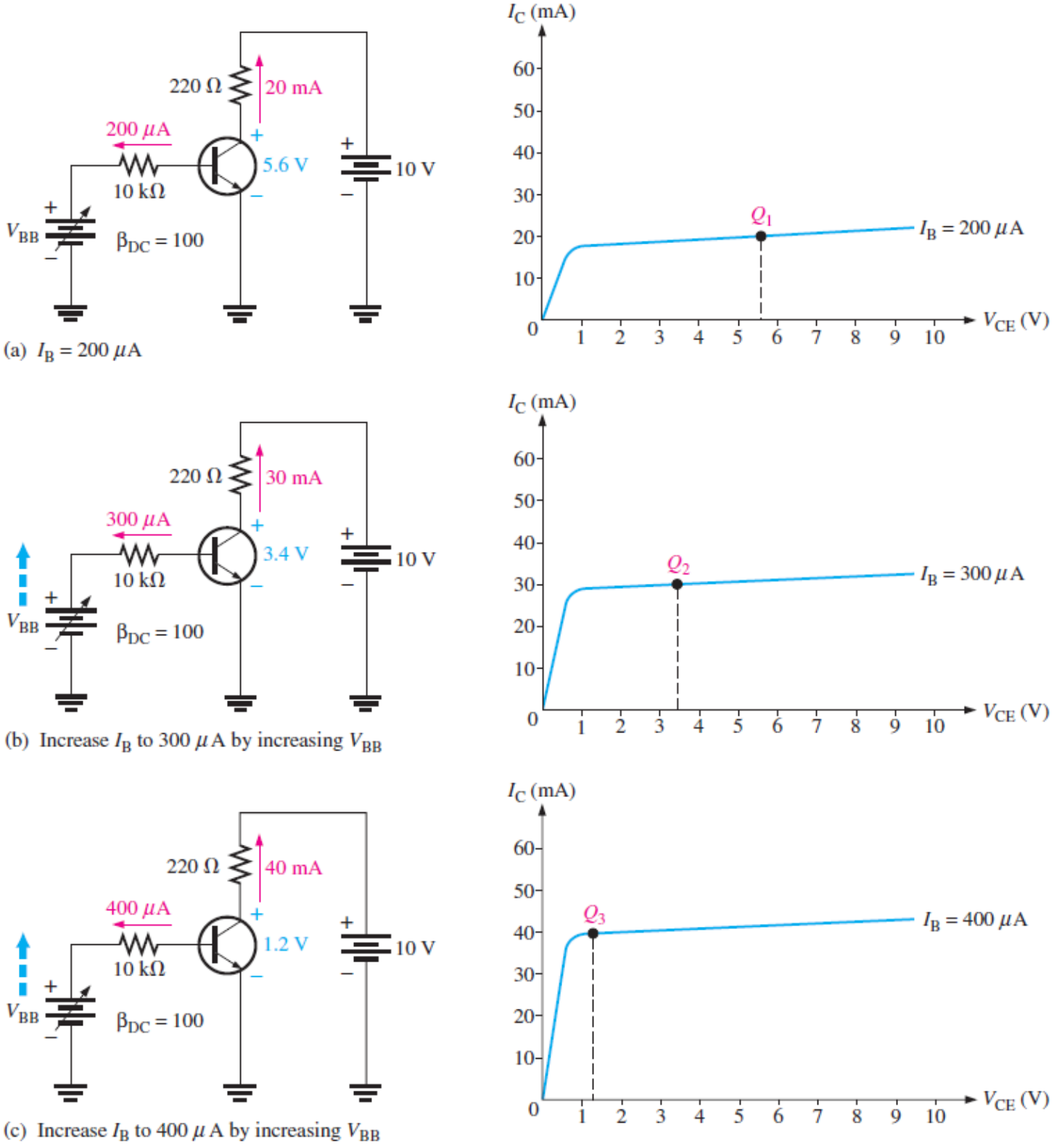


FIGURE 5–3: Illustration of Q-point adjustment.

DC Load Line The dc operation of a transistor circuit can be described graphically using a **dc load line**. This is a straight line drawn on the characteristic curves from the saturation value where $I_C = I_{C(sat)}$ on the *y*-axis to the cutoff value where $V_{CE} = V_{CC}$ on the *x*-axis, as shown in Figure

5–4(a). The load line is determined by the external circuit (V_{CC} and R_C), not the transistor itself, which is described by the characteristic curves.

In Figure 5–3, the equation for I_C is

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C} = -\left(\frac{1}{R_C}\right)V_{CE} + \frac{V_{CC}}{R_C}$$

This is the equation of a straight line with a slope of $-1/R_C$, an x intercept of $V_{CE} = V_{CC}$, and a y intercept of V_{CC}/R_C, which is $I_{C(sat)}$.

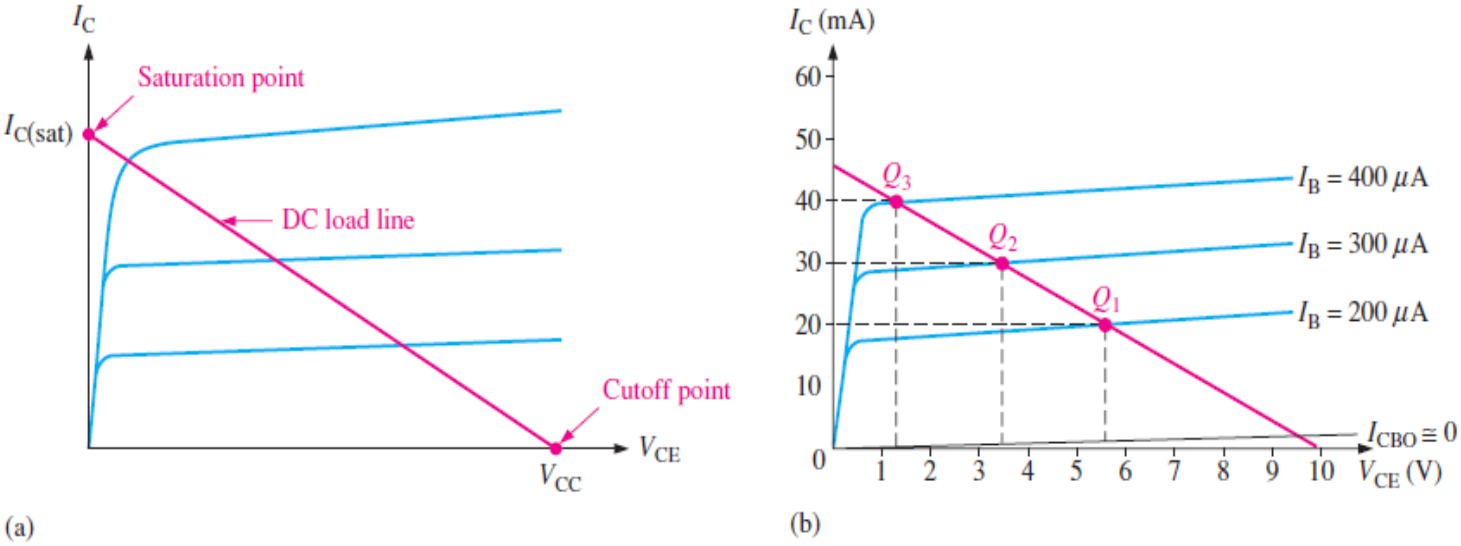
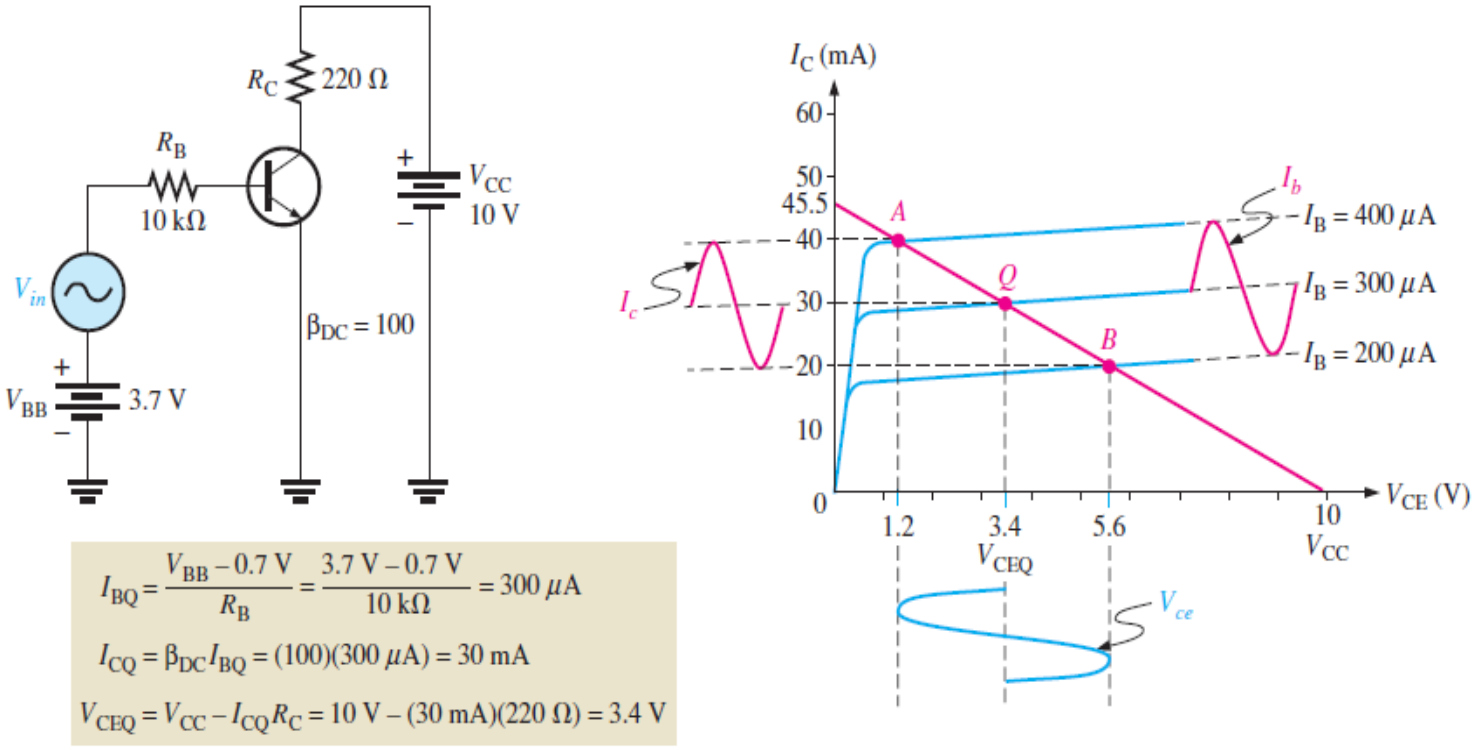


FIGURE 5–4: The dc load line.

The point at which the load line intersects a characteristic curve represents the Q-point for that particular value of I_B. Figure 5– 4(b) illustrates the Q-point on the load line for each value of I_B in Figure 5–3.

Linear Operation The region along the load line including all points between saturation and cutoff is generally known as the **linear region** of the transistor's operation. As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.

Figure 5–5 shows an example of the linear operation of a transistor. AC quantities are indicated by lowercase italic subscripts. Assume a sinusoidal voltage, V_{in}, is superimposed on V_{BB}, causing the base current to vary sinusoidally 100 μA above and below its Q-point value of 300 μA. This, in turn, causes the collector current to vary 10 mA above and below its Q-point value of 30 mA. As a result of the variation in collector current, the collector-to-emitter voltage varies 2.2 V above and below its Q-point value of 3.4 V. Point *A* on the load line in Figure 5–5 corresponds to the positive peak of the sinusoidal input voltage. Point *B* corresponds to the negative peak, and point *Q* corresponds to the zero value of the sine wave, as indicated. V_{CEQ}, I_{CQ}, and I_{BQ} are dc Q-point values with no input sinusoidal voltage applied.



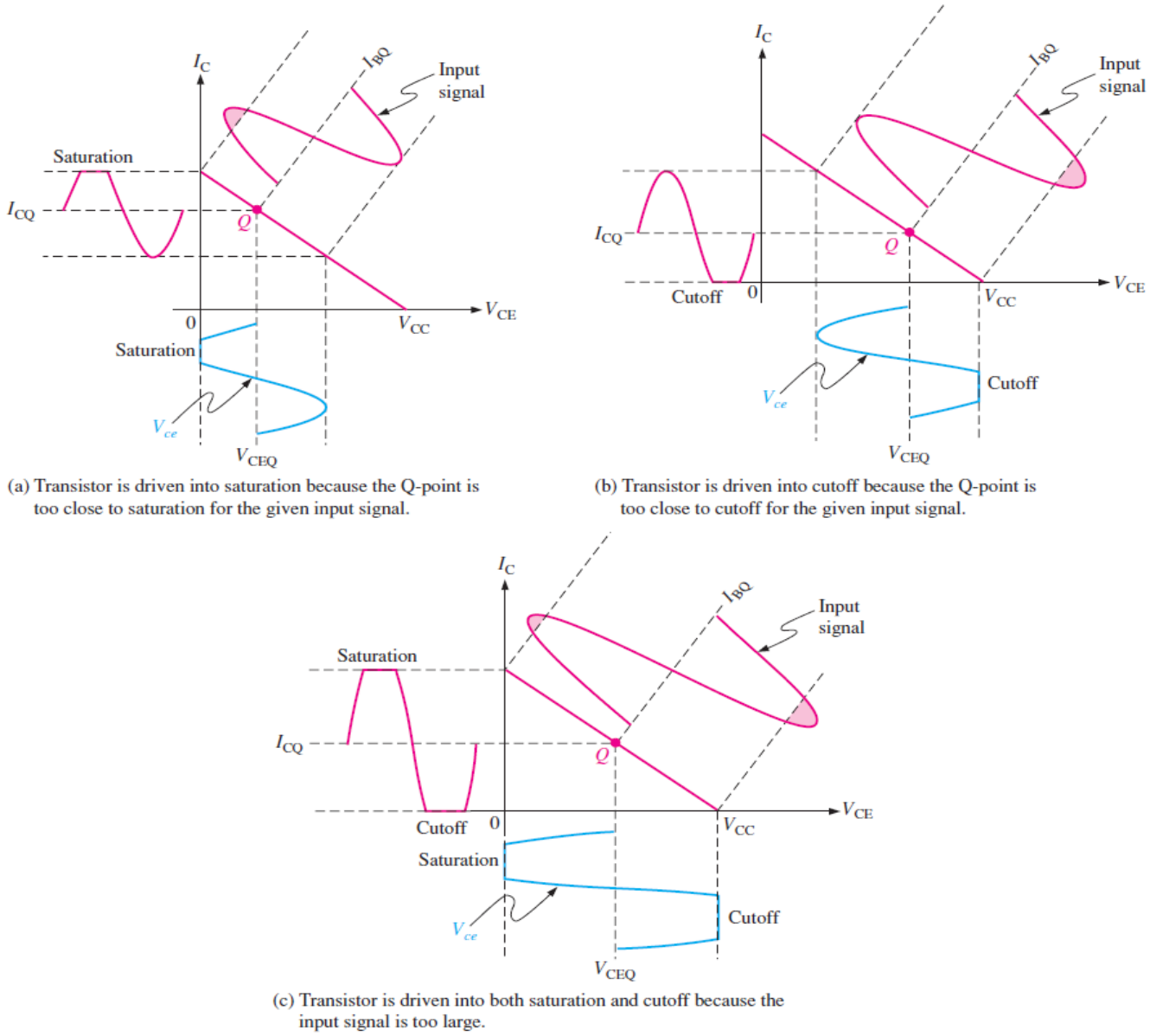
$$I_{BQ} = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3.7\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 300\ \mu\text{A}$$

$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\ \mu\text{A}) = 30\text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 3.4\text{ V}$$

FIGURE 5–5: Variations in collector current and collector-to-emitter voltage as a result of a variation in base current.

Waveform Distortion As previously mentioned, under certain input signal conditions the location of the Q-point on the load line can cause one peak of the V_{ce} waveform to be limited or clipped, as shown in parts (a) and (b) of Figure 5–6. In each case the input signal is too large for the Q-point location and is driving the transistor into cutoff or saturation during a portion of the input cycle. When both peaks are limited as in Figure 5–6(c), the transistor is being driven into both saturation and cutoff by an excessively large input signal. When only the positive peak is limited, the transistor is being driven into cutoff but not saturation. When only the negative peak is limited, the transistor is being driven into saturation but not cutoff.



(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.

(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.

(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

FIGURE 5–6: Graphical load line illustration of a transistor being driven into saturation and/or cutoff.

EXAMPLE 5–1: Determine the Q-point for the circuit in Figure 5–7 and draw the dc load line. Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 200$.

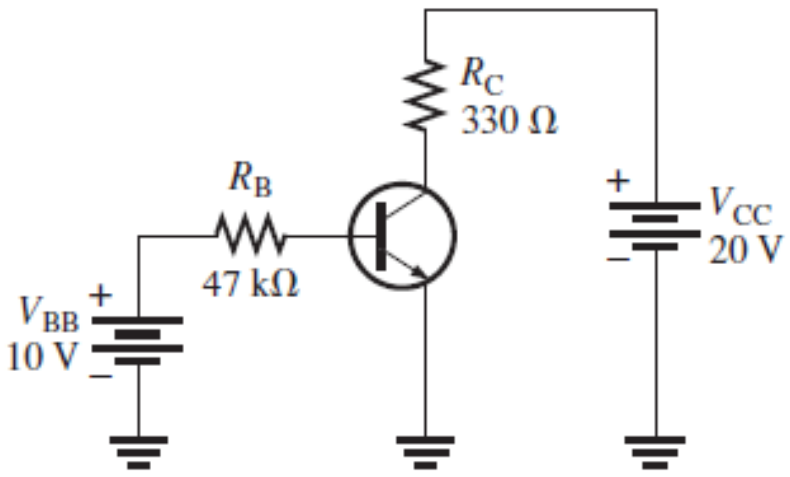


FIGURE 5–7

Solution The Q-point is defined by the values of I_C and V_{CE}.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{47\text{ k}\Omega} = 198\,\mu\text{A}$$

$$I_C = \beta_{DC} I_B = (200)(198\,\mu\text{A}) = 39.6\text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - (39.6\text{ mA})(330\,\Omega) = 10\text{ V} - 13.07\text{ V} = 6.93\text{ V}$$

The Q-point is at $I_C = 39.6$ mA and at $V_{CE} = 6.93$ V.

Since $I_{C(cutoff)} = 0$, we need to know $I_{C(sat)}$ to determine how much variation in collector current can occur and still maintain linear operation of the transistor.

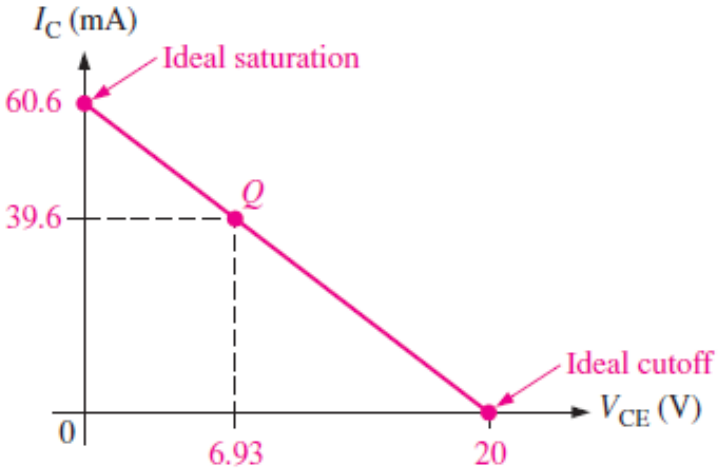
$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20\text{ V}}{330\,\Omega} = 60.6\text{ mA}$$

The dc load line is graphically illustrated in Figure 5–8, showing that before saturation is reached, I_C can increase an amount ideally equal to

$$I_{C(sat)} - I_{CQ} = 60.6\text{ mA} - 39.6\text{ mA} = 21.0\text{ mA}$$

However, I_C can decrease by 39.6 mA before cutoff ($I_C = 0$) is reached. Therefore, the limiting excursion is 21 mA because the *Q-point is closer to saturation than to cutoff.* The 21 mA is the maximum peak variation of the collector current. Actually, it would be slightly less in practice because $V_{CE(sat)}$ is not quite zero.

FIGURE 5–8



Determine the maximum peak variation of the base current as follows:

$$I_{b(peak)} = \frac{I_{c(peak)}}{\beta_{DC}} = \frac{21\text{ mA}}{200} = 105\,\mu\text{A}$$

Related Problem Find the Q-point for the circuit in Figure 5–7, and determine the maximum peak value of base current for linear operation for the following circuit values: $\beta_{DC} = 100$, $R_C = 1.0\text{ k}\Omega$, and $V_{CC} = 24$ V.

5.2 Voltage-Divider Bias

We will now study a method of biasing a transistor for linear operation using a single-source resistive voltage divider. This is the most widely used biasing method. Four other methods are covered in Section 5–3.

Up to this point a separate dc source, V_{BB}, was used to bias the base-emitter junction because it could be varied independently of V_{CC} and it helped to illustrate transistor operation. A more practical bias method is to use V_{CC} as the single bias source, as shown in Figure 5–9. To simplify the schematic, the battery symbol is omitted and replaced by a line termination circle with a voltage indicator (V_{CC}) as shown.

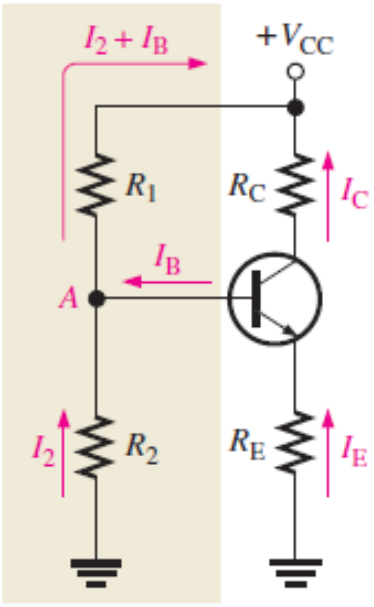


FIGURE 5–9: Voltage-divider bias.

A dc bias voltage at the base of the transistor can be developed by a resistive voltage-divider that consists of R_1 and R_2, as shown in Figure 5–9. V_{CC} is the dc collector supply voltage. Two current paths are between point A and ground: one through R_2 and the other through the base-emitter junction of the transistor and R_E.

Generally, voltage-divider bias circuits are designed so that the base current is much smaller than the current (I_2) through R_2 in Figure 5–9. In this case, the voltage-divider circuit is very straightforward to analyze because the loading effect of the base current can be ignored. A voltage divider in which the base current is small compared to the current in R_2 is said to be a **stiff voltage divider** because the base voltage is relatively independent of different transistors and temperature effects.

To analyze a voltage-divider circuit in which I_B is small compared to I_2, first calculate the voltage on the base using the unloaded voltage-divider rule:

$$\boldsymbol{V_B \cong \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}} \qquad \text{Equation 5–1}$$

Once we know the base voltage, we can find the voltages and currents in the circuit, as follows:

$$\boldsymbol{V_E = V_B - V_{BE}} \qquad \text{Equation 5–2}$$

and

$$\boldsymbol{I_C \cong I_E = \frac{V_E}{R_E}} \qquad \text{Equation 5–3}$$

Then,

$$\boldsymbol{V_C = V_{CC} - I_C R_C} \qquad \text{Equation 5–4}$$

Once we know V_C and V_E, you can determine V_{CE}.

$$V_{CE} = V_C - V_E$$

EXAMPLE 5–2: Determine V_{CE} and I_C in the stiff voltage-divider biased transistor circuit of Figure 5–10 if $\beta_{DC} = 100$.

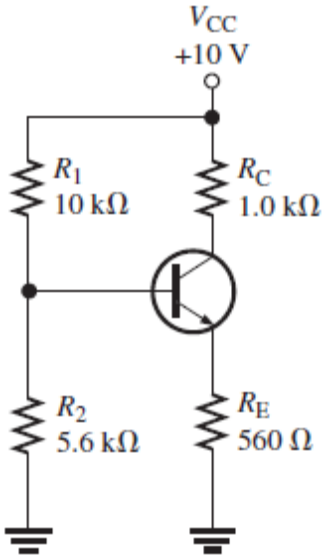


FIGURE 5–10

Solution The base voltage is

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} = \left(\frac{5.6\ \text{k}\Omega}{15.6\ \text{k}\Omega}\right) 10\ \text{V} = 3.59\ \text{V}$$

So,

$$V_E = V_B - V_{BE} = 3.59\ \text{V} - 0.7\ \text{V} = 2.89\ \text{V}$$

And

$$I_E = \frac{V_E}{R_E} = \frac{2.89\ \text{V}}{560\ \Omega} = 5.16\ \text{mA}$$

Therefore,

$$I_C \cong I_E = 5.16\ \text{mA}$$

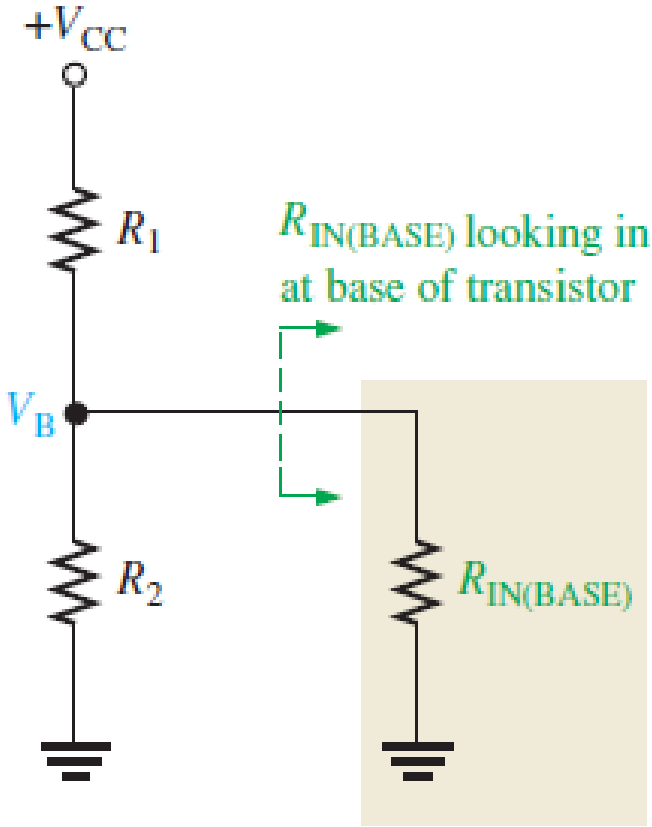
And

$$V_C = V_{CC} - I_C R_C = 10\ \text{V} - (5.16\ \text{mA})(1.0\ \text{k}\Omega) = 4.84\ \text{V}$$

$$V_{CE} = V_C - V_E = 4.84\ \text{V} - 2.89\ \text{V} = 1.95\ \text{V}$$

Related Problem If the voltage divider in Figure 5–10 was not stiff, how would V_B be affected?

The basic analysis developed in Example 5–2 is all that is needed for most voltage-divider circuits, but there may be cases where we need to analyze the circuit with more accuracy. Ideally, a voltage-divider circuit is stiff, which means that the transistor does not appear as a significant load. All circuit design involves trade-offs; and one trade-off is that stiff voltage dividers require smaller resistors, which are not always desirable because of potential loading effects on other circuits and added power requirements. If the circuit designer wanted to raise the input resistance, the divider string may not be stiff; and more detailed analysis is required to calculate circuit parameters. To determine if the divider is stiff, we need to examine the dc input resistance looking in at the base as shown in Figure 5–11.



Stiff:

$$R_{IN(BASE)} \geqq 10R_2$$

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

Not stiff:

$$R_{IN(BASE)} < 10R_2$$

$$V_B = \left(\frac{R_2 \parallel R_{IN(BASE)}}{R_1 + R_2 \parallel R_{IN(BASE)}}\right) V_{CC}$$

FIGURE 5–11: Voltage divider with load.

Loading Effects of Voltage-Divider Bias

DC Input Resistance at the Transistor Base The dc input resistance of the transistor is proportional to β_{DC} so it will change for different transistors. When a transistor is operating in its linear region, the emitter current (I_E) is $\beta_{DC}I_B$. When the emitter resistor is viewed from the base circuit, the resistor appears to be larger than its actual value because of the dc current gain in the transistor. That is, $R_{IN(BASE)} = V_B/I_B = V_B/(I_E/\beta_{DC})$.

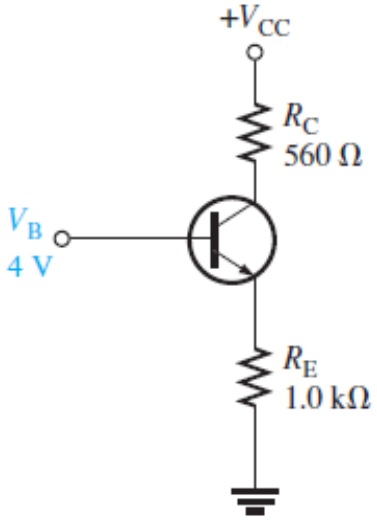
$$\boldsymbol{R_{IN(BASE)} = \frac{\beta_{DC}V_B}{I_E}} \qquad \text{Equation 5–5}$$

This is the effective load on the voltage divider illustrated in Figure 5–11.

We can quickly estimate the loading effect by comparing $R_{IN(BASE)}$ to the resistor R_2 in the voltage divider. As long as $R_{IN(BASE)}$ is at least ten times larger than R_2, the loading effect will be 10% or less and the voltage divider is stiff. If $R_{IN(BASE)}$ is less than ten times R_2, it should be combined in parallel with R_2.

EXAMPLE 5–3: Determine the dc input resistance looking in at the base of the transistor in Figure 5–12. $\beta_{DC} = 125$ and V_B = 4 V.

FIGURE 5–12



Solution

$$V_{BE} = V_B - V_E$$

$$0.7\text{ V} = V_B - I_E R_E$$

$$I_E = \frac{V_B - 0.7\text{ V}}{R_E} = \frac{4\text{ V} - 0.7\text{ V}}{1.0\text{ k}\Omega} = 3.3\text{ mA}$$

$$R_{IN(BASE)} = \frac{\beta_{DC}V_B}{I_E} = \frac{125\text{ V}(4\text{ V})}{3.3\text{ mA}} = 152\text{ k}\Omega$$

Related Problem What is $R_{IN(BASE)}$ in Figure 5–12 if $\beta_{DC} = 60$ and $V_B = 2$ V?

Thevenin's Theorem Applied to Voltage-Divider Bias

To analyze a voltage-divider biased transistor circuit for base current loading effects, we will apply Thevenin's theorem to evaluate the circuit. First, let's get an equivalent base-emitter circuit for the circuit in Figure 5–13(a) using Thevenin's theorem. Looking out from the base terminal, the bias circuit can be redrawn as shown in Figure 5–13(b). Apply Thevenin's theorem to the circuit left of point *A*, with V_{CC} replaced by a short to ground and the transistor disconnected from the circuit. The voltage at point *A* with respect to ground is

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

and the resistance is

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

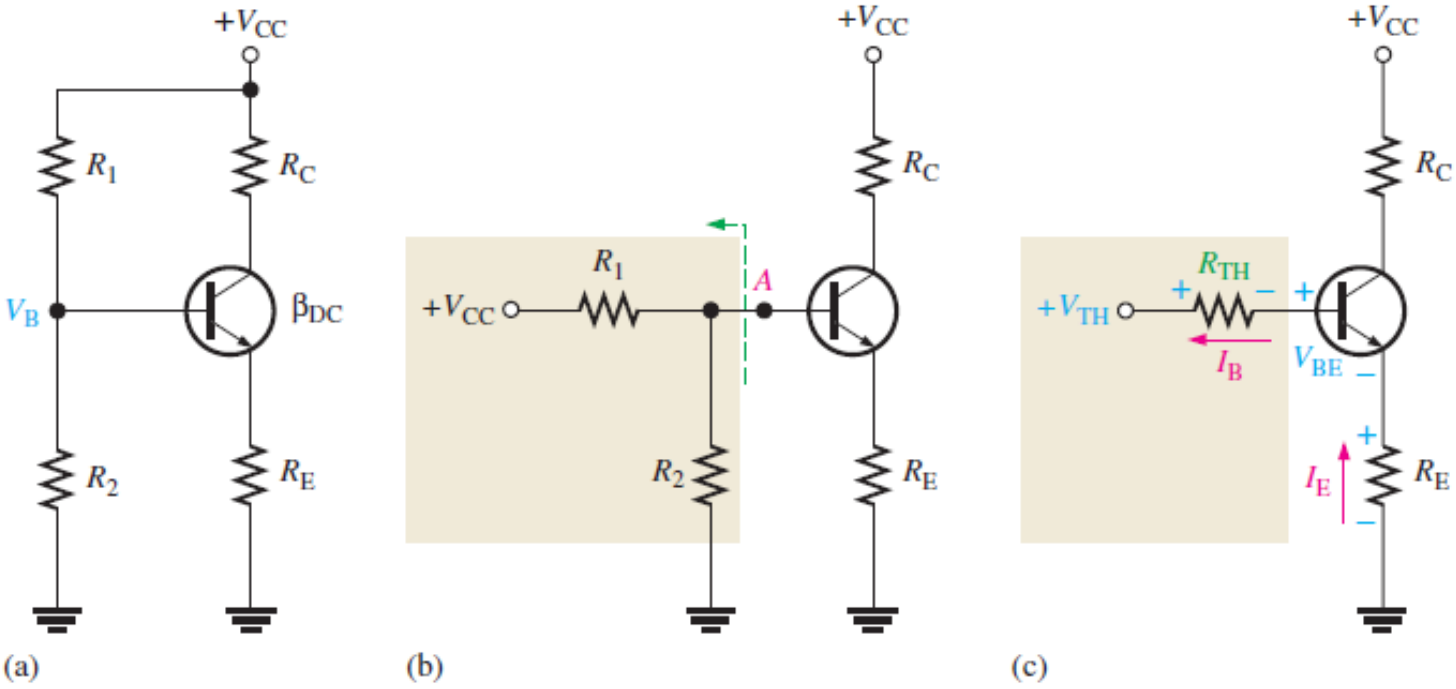


FIGURE 5–13: Thevenizing the bias circuit.

The Thevenin equivalent of the bias circuit, connected to the transistor base, is shown in the beige box in Figure 5–13(c). Applying Kirchhoff's voltage law around the equivalent base-emitter loop gives

$$V_{TH} - V_{R_{TH}} - V_{BE} - V_{R_E} = 0$$

Substituting, using Ohm's law, and solving for V_{TH},

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

Substituting

$$I_B = \frac{I_E}{\beta_{DC}}$$

So,

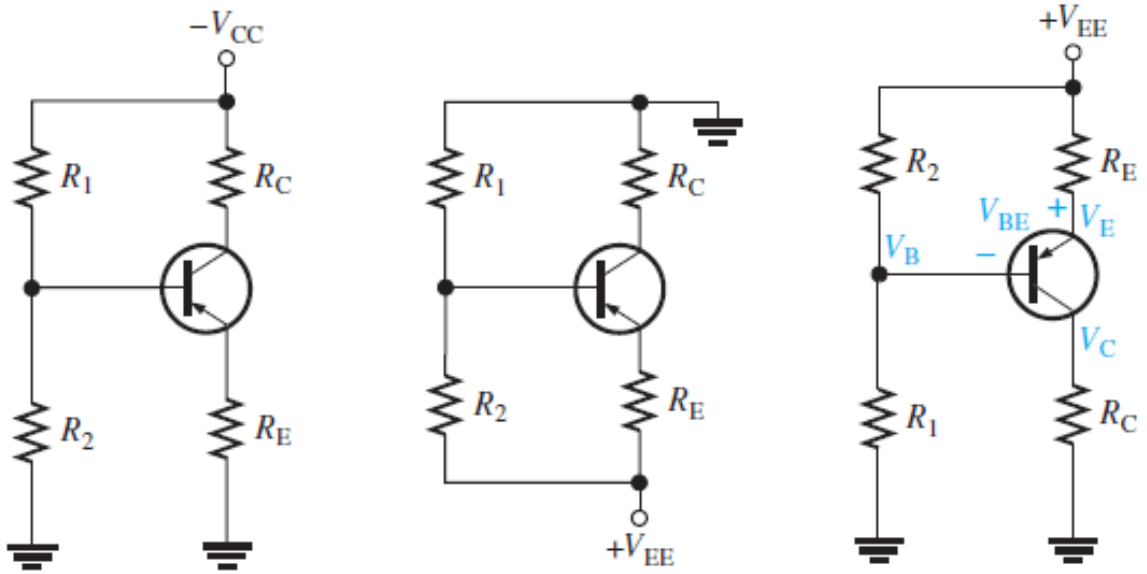
$$V_{TH} = I_E(R_E + R_{TH}/\beta_{DC}) + V_{BE}$$

Then solving for I_E,

$$\boldsymbol{I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}} \qquad \text{Equation 5–6}$$

If R_{TH}/β_{DC} is small compared to R_E, the result is the same as for an unloaded voltage divider. Voltage-divider bias is widely used because reasonably good bias stability is achieved with a single supply voltage.

Voltage-Divider Biased PNP Transistor As we know, a *pnp* transistor requires bias polarities opposite to the *npn.* This can be accomplished with a negative collector supply voltage, as in Figure 5–14(a), or with a positive emitter supply voltage, as in Figure 5–14(b).



(a) Negative collector supply voltage, V_{CC} (b) Positive emitter supply voltage, V_{EE} (c) The circuit in (b) redrawn

FIGURE 5–14: Voltage-divider biased *pnp* transistor.

In a schematic, the *pnp* is often drawn upside down so that the supply voltage is at the top of the schematic and ground at the bottom, as in Figure 5–14(c).

The analysis procedure is the same as for an *npn* transistor circuit using Thevenin's theorem and Kirchhoff's voltage law, as demonstrated in the following steps with reference to Figure 5–14. For Figure 5–14(a), applying Kirchhoff's voltage law around the base-emitter circuit gives

$$V_{TH} + I_B R_{TH} - V_{BE} + I_E R_E = 0$$

By Thevenin's theorem,

$$V_{\text{TH}} = \left(\frac{R_2}{R_1 + R_2}\right) V_{\text{CC}}$$

$$R_{\text{TH}} = \frac{R_1 R_2}{R_1 + R_2}$$

The base current is

$$I_{\text{B}} = \frac{I_{\text{E}}}{\beta_{\text{DC}}}$$

The equation for I_{E} is

$$\boldsymbol{I_{\text{E}} = \frac{-V_{\text{TH}} + V_{\text{BE}}}{R_{\text{E}} + R_{\text{TH}}/\beta_{\text{DC}}}} \qquad \text{Equation 5–7}$$

For Figure 5–14(b), the analysis is as follows:

$$-V_{\text{TH}} + I_{\text{B}} R_{\text{TH}} - V_{\text{BE}} + I_{\text{E}} R_{\text{E}} - V_{\text{EE}} = 0$$

$$V_{\text{TH}} = \left(\frac{R_1}{R_1 + R_2}\right) V_{\text{EE}}$$

$$R_{\text{TH}} = \frac{R_1 R_2}{R_1 + R_2}$$

$$I_{\text{B}} = \frac{I_{\text{E}}}{\beta_{\text{DC}}}$$

The equation for I_{E} is

$$\boldsymbol{I_{\text{E}} = \frac{V_{\text{TH}} + V_{\text{BE}} - V_{\text{EE}}}{R_{\text{E}} + R_{\text{TH}}/\beta_{\text{DC}}}} \qquad \text{Equation 5–8}$$

EXAMPLE 5–4: Find I_C and V_{EC} for the *pnp* transistor circuit in Figure 5–15.

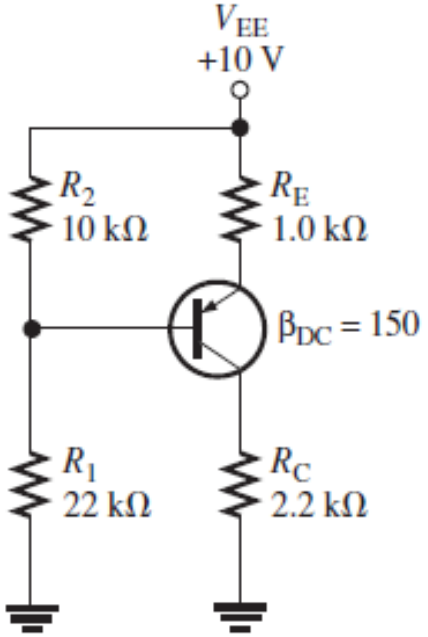


FIGURE 5–15

Solution This circuit has the configuration of Figures 5–14(b) and (c). Apply Thevenin's theorem.

$$V_{\text{TH}} = \left(\frac{R_1}{R_1 + R_2}\right) V_{\text{EE}} = \left(\frac{22\ \text{k}\Omega}{22\ \text{k}\Omega + 10\ \text{k}\Omega}\right) 10\ \text{V} = (0.688)10\ \text{V} = 6.88\ \text{V}$$

$$R_{\text{TH}} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(22\ \text{k}\Omega)(10\ \text{k}\Omega)}{22\ \text{k}\Omega + 10\ \text{k}\Omega} = 6.88\ \text{k}\Omega$$

Use Equation 5–8 to determine I_{E}.

$$I_{\text{E}} = \frac{V_{\text{TH}} + V_{\text{BE}} - V_{\text{EE}}}{R_{\text{E}} + R_{\text{TH}}/\beta_{\text{DC}}} = \frac{6.88\ \text{V} + 0.7\ \text{V} - 10\ \text{V}}{1.0\ \text{k}\Omega + 6.88\ \text{k}\Omega/150} = \frac{-2.42\ \text{V}}{1.0\ \text{k}\Omega + 45.9\ \Omega} = -2.31\ \text{mA}$$

The negative sign on I_{E} indicates that the assumed current direction in the Kirchhoff's analysis is opposite from the actual current direction. From I_{E}, we can determine I_{C} and V_{EC} as follows:

$$I_{\text{C}} = I_{\text{E}} = 2.31\ \text{mA}$$

$$V_{\text{C}} = I_{\text{C}} R_{\text{C}} = (2.31\ \text{mA})(2.2\ \text{k}\Omega) = 5.08\ \text{V}$$

$$V_{\text{E}} = V_{\text{EE}} - V_{R_{\text{E}}} = V_{\text{EE}} - I_{\text{E}} R_{\text{E}} = 10\ \text{V} - (2.31\ \text{mA})(1.0\ \text{k}\Omega) = 7.68\ \text{V}$$

$$V_{\text{EC}} = V_{\text{E}} - V_{\text{C}} = 7.68\ \text{V} - 5.08\ \text{V} = 2.6\ \text{V}$$

Related Problem Determine $R_{\text{IN(BASE)}}$ for Figure 5–15.

EXAMPLE 5–5: Find I_{C} and V_{CE} for a *pnp* transistor circuit with these values: $R_1 = 68\ \text{k}\Omega$, $R_2 = 47\ \text{k}\Omega$, $R_{\text{C}} = 1.8\ \text{k}\Omega$, $R_{\text{E}} = 2.2\ \text{k}\Omega$, $V_{\text{CC}} = -6\ \text{V}$, and $\beta_{\text{DC}} = 75$. Refer to Figure 5–14(a), which shows the schematic with a negative supply voltage.

Solution Apply Thevenin's theorem.

$$V_{\text{TH}} = \left(\frac{R_2}{R_1 + R_2}\right) V_{\text{CC}} = \left(\frac{47\ \text{k}\Omega}{68\ \text{k}\Omega + 47\ \text{k}\Omega}\right)(-6\ \text{V}) = (0.409)(-6\ \text{V}) = -2.45\ \text{V}$$

$$R_{\text{TH}} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(68\ \text{k}\Omega)(47\ \text{k}\Omega)}{68\ \text{k}\Omega + 47\ \text{k}\Omega} = 27.8\ \text{k}\Omega$$

Use Equation 5–7 to determine I_{E}.

$$I_{\text{E}} = \frac{-V_{\text{TH}} + V_{\text{BE}}}{R_{\text{E}} + R_{\text{TH}}/\beta_{\text{DC}}} = \frac{-(-2.45\ \text{V}) + 0.7\ \text{V}}{2.2\ \text{k}\Omega + 27.8\ \text{k}\Omega/75} = \frac{3.15\ \text{V}}{2.2\ \text{k}\Omega + 371\ \Omega} = 1.23\ \text{mA}$$

From I_{E}, we can determine I_{C} and V_{CE} as follows:

$$I_C = I_E = 1.23\ \text{mA}$$

$$V_C = -V_{CC} - V_{R_C} = -V_{CC} + I_C R_C = -6\ \text{V} + (1.23\ \text{mA})(1.8\ \text{k}\Omega) = -3.79\ \text{V}$$

$$V_E = V_{EE} - V_{R_E} = V_{EE} - I_E R_E = 0 - (1.23\ \text{mA})(2.2\ \text{k}\Omega) = -2.71\ \text{V}$$

$$V_{CE} = V_C - V_E = -3.79\ \text{V} - (-2.71\ \text{V}) = -1.08\ \text{V}$$

Related Problem What value of β_{DC} is required in this example in order to neglect $R_{IN(BASE)}$) in keeping with the basic ten-times rule for a stiff voltage divider?

5.3 Other Bias Methods

In this section, four additional methods for dc biasing a transistor circuit are discussed. Although these methods are not as common as voltage-divider bias, we should be able to recognize them when we see them and understand the basic differences.

Emitter Bias

Emitter bias provides excellent bias stability in spite of changes in β or temperature. It uses both a positive and a negative supply voltage. To obtain a reasonable estimate of the key dc values in an emitter-biased circuit, analysis is quite easy. In an *npn* circuit, such as shown in Figure 5–17, the small base current causes the base voltage to be slightly below ground. The emitter voltage is one diode drop less than this. The combination of this small drop across R_B and V_{BE} forces the emitter to be at approximately -1 V. Using this approximation, we can obtain the emitter current as

$$I_E = \frac{-V_{EE} - 1\ \text{V}}{R_E}$$

V_{EE} is entered as a negative value in this equation.

We can apply the approximation that $I_C \cong I_E$ to calculate the collector voltage.

$$V_C = V_{CC} - V_{R_C} = V_{CC} - I_C R_C$$

The approximation that $V_E = -1$ V is useful for troubleshooting because we won't need to perform any detailed calculations. As in the case of voltage-divider bias, there is a more rigorous calculation for cases where we need a more exact result.

The approximation that $V_E = -1$ V and the neglect of β_{DC} may not be accurate enough for design work or detailed analysis. In this case, Kirchhoff's voltage law can be applied as follows to develop a more detailed formula for I_E. Kirchhoff's voltage law applied around the base-emitter

circuit in Figure 5–17(a), which has been redrawn in part (b) for analysis, gives the following equation:

$$V_{EE} + V_{R_B} + V_{BE} + V_{R_E} = 0$$

Substituting, using Ohm's law,

$$V_{EE} + I_B R_B + V_{BE} + I_E R_E = 0$$

Substituting $I_B \cong I_E/\beta_{DC}$ for and transposing V_{EE},

$$\left(\frac{I_E}{\beta_{DC}}\right) R_B + I_E R_E + V_{BE} = -V_{EE}$$

Factoring out I_E and solving for I_E,

$$\boldsymbol{I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}}} \qquad \text{Equation 5–9}$$

Voltages with respect to ground are indicated by a single subscript. The emitter voltage with respect to ground is

$$V_E = V_{EE} + V_{R_E} = V_{EE} + I_E R_E$$

The base voltage with respect to ground is

$$V_B = V_E + V_{BE}$$

The collector voltage with respect to ground is

$$V_C = V_{CC} - V_{R_C} = V_{CC} - I_C R_C$$

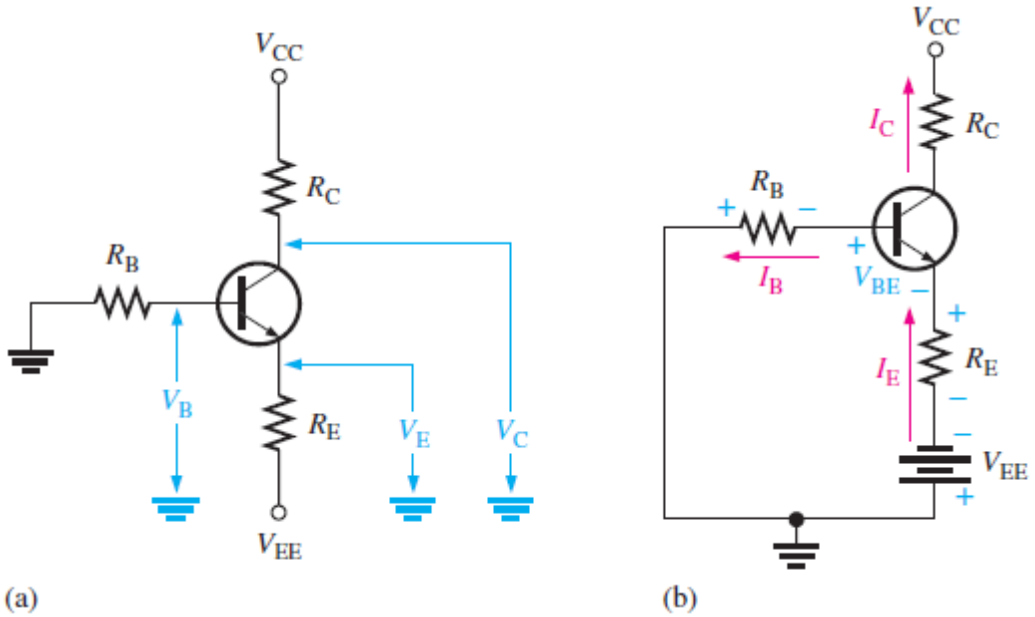
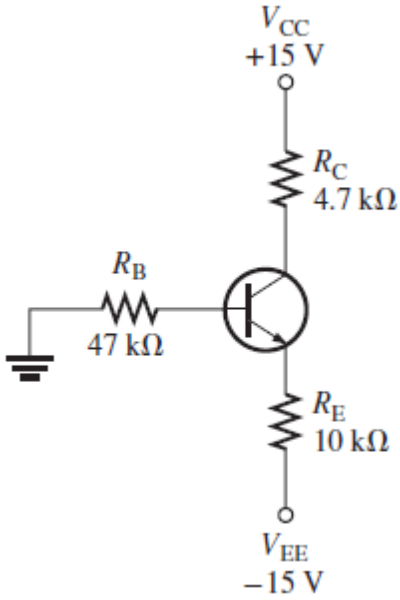


FIGURE 5–17: An *npn* transistor with emitter bias. Polarities are reversed for a *pnp* transistor. Single subscripts indicate voltages with respect to ground.

EXAMPLE 5–6: Calculate I_E and V_{CE} for the circuit in Figure 5–16 using the approximations $V_E \cong -1$ V and $I_C \cong I_E$.

FIGURE 5–16



Solution

$$V_E \cong -1 \text{ V}$$

$$I_E = \frac{-V_{EE} - 1 \text{ V}}{R_E} = \frac{-(-15 \text{ V}) - 1 \text{ V}}{10 \text{ k}\Omega} = \frac{14 \text{ V}}{10 \text{ k}\Omega} = 1.4 \text{ mA}$$

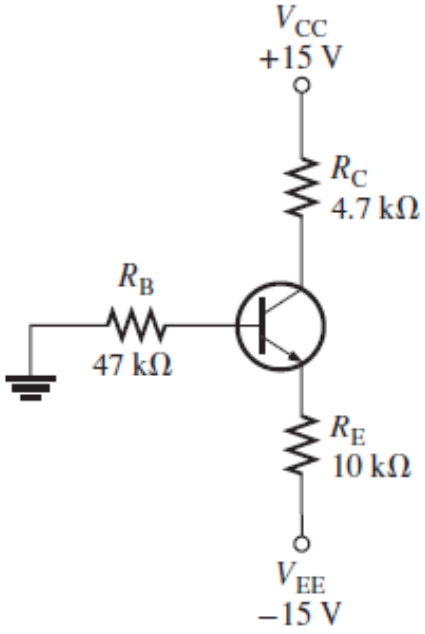
$$V_C = V_{CC} - V_{R_C} = V_{CC} - I_C R_C = +15 \text{ V} - (1.4 \text{ mA})(4.7 \text{ k}\Omega) = 8.4 \text{ V}$$

$$V_{CE} = V_C - V_E = 8.4 \text{ V} - (-1 \text{ V}) = 9.4 \text{ V}$$

Related Problem If V_{CE} is changed to -12 V, what is the new value of V_{CE}?

EXAMPLE 5–7: Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–18 will change if β_{DC} increases from 100 to 200 when one transistor is replaced by another.

FIGURE 5–18



Solution For $\beta_{DC} = 100$,

$$I_{C(1)} \cong I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{-(-15\text{V}) - 0.7\text{ V}}{10\text{ k}\Omega + 47\text{ k}\Omega/100} = 1.37\text{ mA}$$

$$V_C = V_{CC} - I_{C(1)}R_C = 15\text{ V} - (1.37\text{ mA})(4.7\text{ k}\Omega) = 8.56\text{ V}$$

$$V_E = V_{EE} + I_E R_E = -15\text{ V} + (1.37\text{ mA})(10\text{ k}\Omega) = -1.3\text{ V}$$

Therefore,

$$V_{CE(1)} = V_C - V_E = 8.56\text{ V} - (-1.3) = 9.83\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} \cong I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{-(-15\text{V}) - 0.7\text{ V}}{10\text{ k}\Omega + 47\text{ k}\Omega/200} = 1.38\text{ mA}$$

$$V_C = V_{CC} - I_{C(2)}R_C = 15\text{ V} - (1.38\text{ mA})(4.7\text{ k}\Omega) = 8.51\text{ V}$$

$$V_E = V_{EE} + I_E R_E = -15\text{ V} + (1.38\text{ mA})(10\text{ k}\Omega) = -1.2\text{ V}$$

Therefore,

$$V_{CE(2)} = V_C - V_E = 8.51\text{ V} - (-1.2) = 9.71\text{ V}$$

The percent change in I_C as β_{DC} changes from 100 to 200 is

$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right) 100\% = \left(\frac{1.38\text{ mA} - 1.37\text{ mA}}{1.37\text{ mA}}\right) 100\% = 0.730\%$$

The percent change in V_{CE} is

$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right) 100\% = \left(\frac{9.71\text{ V} - 9.83\text{ V}}{9.83\text{ V}}\right) 100\% = -1.22\%$$

Related Problem Determine the Q-point in Figure 5–18 if β_{DC} increases to 300.

Base Bias

This method of biasing is common in switching circuits. Figure 5–19 shows a base-biased transistor. The analysis of this circuit for the linear region shows that it is directly dependent on β_{DC}. Starting with Kirchhoff's voltage law around the base circuit,

$$V_{CC} - V_{R_B} - V_{BE} = 0$$

Substituting $I_B R_B$ for V_{R_B} we get

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Then solving for I_B,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Kirchhoff's voltage law applied around the collector circuit in Figure 5–19 gives the following equation:

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Solving for V_{CE},

$$V_{CE} = V_{CC} - I_C R_C \qquad \text{Equation 5–10}$$

Substituting the expression for I_B into the formula $I_C = \beta_{DC} I_B$ yields

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) \qquad \text{Equation 5–11}$$

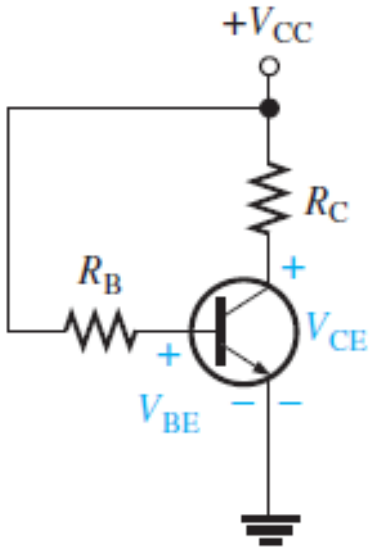


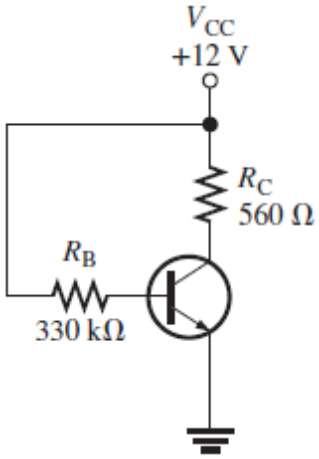
FIGURE 5–19: Base bias.

Q-Point Stability of Base Bias Notice that Equation 5–11 shows that I_C is dependent onβ_{DC}. The disadvantage of this is that a variation in β_{DC} causes I_C and, as a result, V_{CE} to change, thus changing the Q-point of the transistor. This makes the base bias circuit extremely beta-dependent and unpredictable.

Recall that β_{DC} varies with temperature and collector current. In addition, there is a large spread of β_{DC} values from one transistor to another of the same type due to manufacturing variations. For these reasons, base bias is rarely used in linear circuits but is discussed here so we will be familiar with it.

EXAMPLE 5–8: Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–20 will change over a temperature range where β_{DC} increases from 100 to 200.

FIGURE 5–20



Solution

For $\beta_{DC} = 100$,

$$I_{C(1)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 100\left(\frac{12\text{ V} - 0.7\text{ V}}{330\text{ k}\Omega}\right) = 3.42\text{ mA}$$

$$V_{CE(1)} = V_{CC} - I_{C(1)}R_C = 12\text{ V} - (3.42\text{ mA})(560\ \Omega) = 10.1\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 200\left(\frac{12\text{ V} - 0.7\text{ V}}{330\text{ k}\Omega}\right) = 6.84\text{ mA}$$

$$V_{CE(2)} = V_{CC} - I_{C(2)}R_C = 12\text{ V} - (6.84\text{ mA})(560\ \Omega) = 8.17\text{ V}$$

The percent change in I_C as β_{DC} changes from 100 to 200 is

$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right)100\% = \left(\frac{6.84\text{ mA} - 3.42\text{ mA}}{3.42\text{ mA}}\right)100\% = 100\%\ \text{(an increase)}$$

The percent change in V_{CE} is

$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right)100\% = \left(\frac{8.17\text{ V} - 10.1\text{ V}}{10.1\text{ V}}\right)100\% = -19.1\%\ \text{(a decrease)}$$

As we can see, the Q-point is very dependent on β_{DC} in this circuit and therefore makes the base bias arrangement very unreliable. Consequently, base bias is not normally used if linear operation is required. However, it can be used in switching applications.

Related Problem Determine I_C if β_{DC} increases to 300.

Emitter-Feedback Bias

If an emitter resistor is added to the base-bias circuit in Figure 5–20, the result is emitter-feedback bias, as shown in Figure 5–21. The idea is to help make base bias more predictable with negative **feedback**, which negates any attempted change in collector current with an opposing change in base voltage. If the collector current tries to increase, the emitter voltage increases, causing an increase in base voltage because $V_B = V_E + V_{BE}$. This increase in base voltage reduces the voltage across R_B, thus reducing the base current and keeping the collector current from increasing. A similar action occurs if the collector current tries to decrease. While this is better for linear circuits than base bias, it is still dependent on β_{DC} and is not as predictable as voltage-divider bias. To calculate I_E, we can write Kirchhoff's voltage law (KVL) around the base circuit.

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$$

Substituting I_E/β_{DC} for I_B, we can see that I_E is still dependent on β_{DC}.

$$\boldsymbol{I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}}} \qquad \text{Equation 5–12}$$

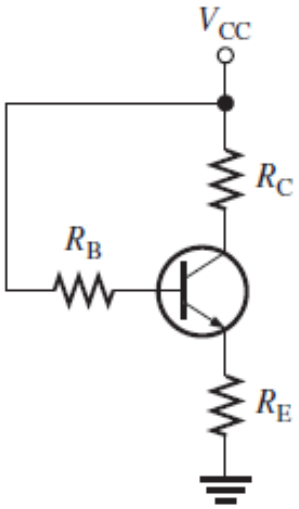


FIGURE 5–21: Emitter-feedback bias.

EXAMPLE 5–9: The base-bias circuit from Example 5–8 is converted to emitter-feedback bias by the addition of a 1 kΩ emitter resistor. All other values are the same, and a transistor with a $\beta_{DC} = 100$ is used. Determine how much the Q-point will change if the first transistor is replaced with one having a $\beta_{DC} = 200$. Compare the results to those of the base-bias circuit.

Solution

For $\beta_{DC} = 100$,

$$I_{C(1)} = I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{12\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega + 330\text{ k}\Omega/100} = 2.63\text{ mA}$$

$$V_{CE(1)} = V_{CC} - I_{C(1)}(R_C + R_E) = 12\text{ V} - (2.63\text{ mA})(560\ \Omega + 1\text{ k}\Omega) = 7.90\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} = I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{12\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega + 330\text{ k}\Omega/200} = 4.26\text{ mA}$$

$$V_{CE(2)} = V_{CC} - I_{C(2)}(R_C + R_E) = 12\text{ V} - (4.26\text{ mA})(560\ \Omega + 1\text{ k}\Omega) = 5.35\text{ V}$$

The percent change in I_C is

$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right) 100\% = \left(\frac{4.26\text{ mA} - 2.63\text{ mA}}{2.63\text{ mA}}\right) 100\% = 62.0\%$$

$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right) 100\% = \left(\frac{5.35\text{ V} - 7.90\text{ V}}{7.90\text{ V}}\right) 100\% = -32.3\%$$

Although the emitter-feedback bias significantly improved the stability of the bias for a change in β_{DC} compared to base bias, it still does not provide a reliable Q-point.

Related Problem Determine I_C if a transistor with $\beta_{DC} = 300$ is used in the circuit.

Collector-Feedback Bias

In Figure 5–22, the base resistor R_B is connected to the collector rather than to V_{CC}, as it was in the base bias arrangement discussed earlier. The collector voltage provides the bias for the base-emitter junction. The negative feedback creates an "offsetting" effect that tends to keep the Q-point stable. If I_C tries to increase, it drops more voltage across R_C, thereby causing V_C to decrease. When V_C decreases, there is a decrease in voltage across R_B, which decreases I_B. The decrease in I_B produces less I_C which, in turn, drops less voltage across R_C and thus offsets the decrease in V_C.

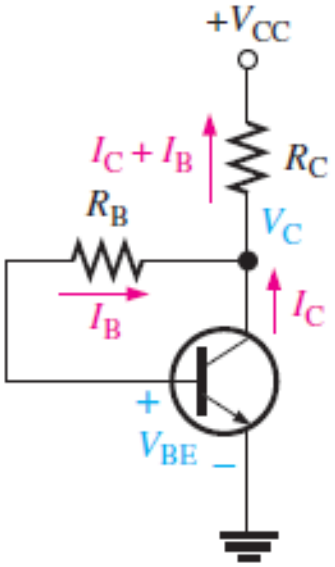


FIGURE 5–22: Collector-feedback bias.

Analysis of a Collector-Feedback Bias Circuit By Ohm's law, the base current can be expressed as

$$I_{\mathrm{B}} = \frac{V_{\mathrm{C}} - V_{\mathrm{BE}}}{R_{\mathrm{B}}}$$

Let's assume that $I_{\mathrm{C}} \gg I_{\mathrm{B}}$. The collector voltage is

$$V_{\mathrm{C}} \cong V_{\mathrm{CC}} - I_{\mathrm{C}}R_{\mathrm{C}}$$

Also,

$$I_{\mathrm{B}} = \frac{I_{\mathrm{C}}}{\beta_{\mathrm{DC}}}$$

Substituting for V_{C} in the equation $I_{\mathrm{B}} = (V_{\mathrm{C}} - V_{\mathrm{BE}})/R_{\mathrm{B}}$,

$$\frac{I_{\mathrm{C}}}{\beta_{\mathrm{DC}}} = \frac{V_{\mathrm{CC}} - I_{\mathrm{C}}R_{\mathrm{C}} - V_{\mathrm{BE}}}{R_{\mathrm{B}}}$$

The terms can be arranged so that

$$\frac{I_{\mathrm{C}}R_{\mathrm{B}}}{\beta_{\mathrm{DC}}} + I_{\mathrm{C}}R_{\mathrm{C}} = V_{\mathrm{CC}} - V_{\mathrm{BE}}$$

Then you can solve for I_{C} as follows:

$$I_{\mathrm{C}}\left(R_{\mathrm{C}} + \frac{R_{\mathrm{B}}}{\beta_{\mathrm{DC}}}\right) = V_{\mathrm{CC}} - V_{\mathrm{BE}}$$

$$I_{\mathrm{C}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{BE}}}{R_{\mathrm{C}} + R_{\mathrm{B}}/\beta_{\mathrm{DC}}} \qquad \text{Equation 5–13}$$

Since the emitter is ground, $V_{\mathrm{CE}} = V_{\mathrm{C}}$.

$$V_{\mathrm{CE}} = V_{\mathrm{CC}} - I_{\mathrm{C}}R_{\mathrm{C}} \qquad \text{Equation 5–14}$$

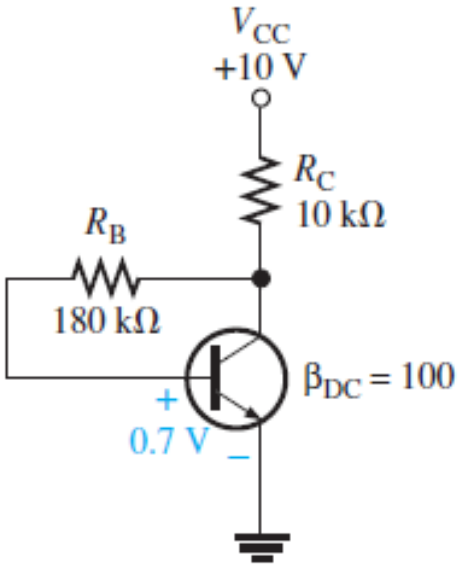
Q-Point Stability Over Temperature Equation 5–13 shows that the collector current is dependent to some extent on β_{DC} and V_{BE}. This dependency, of course, can be minimized by making $R_{\mathrm{C}} \gg R_{\mathrm{B}}/\beta_{\mathrm{DC}}$ and $V_{\mathrm{CC}} \gg V_{\mathrm{BE}}$. An important feature of collector-feedback bias is that it essentially eliminates the β_{DC} and V_{BE} dependency even if the stated conditions are met.

As we have learned, β_{DC} varies directly with temperature, and V_{BE} varies inversely with temperature. As the temperature goes up in a collector-feedback circuit, β_{DC} goes up and V_{BE} goes down. The increase in β_{DC} acts to increase I_{C}. The decrease in V_{BE} acts to increase I_{B} which, in turn also acts to increase I_{C}. As I_{C} tries to increase, the voltage drop across R_{C} also tries to

increase. This tends to reduce the collector voltage and therefore the voltage across R_B, thus reducing I_B and offsetting the attempted increase in I_C and the attempted decrease in V_C. The result is that the collector-feedback circuit maintains a relatively stable Q-point. The reverse action occurs when the temperature decreases.

EXAMPLE 5–10: Calculate the Q-point values (I_C and V_{CE}) for the circuit in Figure 5–23.

FIGURE 5–23



Solution Using Equation 5–13, the collector current is

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta_{DC}} = \frac{10\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega + 180\text{ k}\Omega/100} = 788\,\mu\text{A}$$

Using Equation 5–14, the collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (788\,\mu\text{A})(10\text{ k}\Omega) = 2.12\text{ V}$$

Related Problem Calculate the Q-point values in Figure 5–23 for $\beta_{DC} = 200$ and determine the percent change in the Q-point from $\beta_{DC} = 100$ to $\beta_{DC} = 200$.