MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Logic**			**Module Delivery**	
Module Type	**Core**			☒**Theory** ☒**Lecture** ☒**Lab** ☐**Tutorial** ☐**Practical** ☐**Seminar**	
Module Code	**COM-114**				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level			**Semester of Delivery**	1	
Administering Department	COM		**College**	cos	
Module Leader	Yahiea M.H. Al Naiemy		**e-mail**	Yahiea.alnaiemy@uodiyala.edu.iq	
Module Leader's Acad. Title	Lecturer		**Module Leader's Qualification**	Ph.D.	
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name	Name		**e-mail**	E-mail	
Scientific Committee Approval Date	01/06/2023		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	This is core course of Computer Science Department and that presents basic tools for the design of digital circuits. It serves as a building block in many disciplines that utilize data of digital nature like digital control, data communication, digital computers etc. The goal of this course is to; 1. Perform arithmetic operations in many number systems. 2. Manipulate Boolean algebraic structures. 3. Simplify the Boolean expressions using Karnaugh Map (K-MAP). 4. Implement the Boolean Functions using NAND and NOR gates. 5. Analyze and design various combinational logic circuits such as (Binary Adder and Substructor, Multiplexer, Decoder, Programmable Logic Array (PLA)). 6. Understand the basic functions of Flip-Flops. 7. Understand the importance of state diagram representation of sequential circuits. 8. Analyze and design clocked sequential circuits such as Counters and Registers.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	This course makes significant contributions to the following program outcomes: 1. An ability to apply knowledge of mathematics, science, and engineering, 2. An ability to design and conduct experiments, as well as to analyze and interpret data, 3. An ability to design a system, component , or process to meet desired needs within realistic constraints 4. An ability to identify, formulate, and solve Science and engineering problems, 5. An ability to use the techniques, skills, and modern engineering tools necessary for Computer and Engineering practice.
Indicative Contents المحتويات الإرشادية	1. Digital Systems and Binary Numbers • Digital Systems, • Binary Numbers, • Number-base Conversions, • Octal and Hexadecimal Numbers, • Complements, • Signed Binary Numbers, • Binary Codes, Binary Storage and Registers, • Binary Logic. 2. Boolean Algebra and Logic Gates: • Introduction, • Basic Definitions, • Axiomatic Definition of Boolean Algebra, • Basic Theorems and Properties of Boolean Algebra, • Boolean Functions, • Canonical and Standard Forms, • Other Logic Operations,

	• Digital Logic Gates, • Integrated Circuits. 3. Gate level Minimization: • The Map Method, • Two-variable map, • Three-variable map, • Four-Variable Map, • Five-variable Map, • Product of Sums Simplification, • Don't-care Conditions, • NAND and NOR Implementation, • Other Two-Level Implementations, • Exclusive-OR and NOR Function. 4. Combinational Logic: • Introduction, • Combination Circuits, • Analysis Procedure, • Design Procedure, • Binary Adder-Subtractor, • Decimal Adder, • Binary Multiplier, • Magnitude Comparator, • Decoders, • Encoders, • Multiplexers and DeMultiplexers. 5. Synchronous Sequential Logic: • Introduction, • Sequential Circuits, • Storage Element: • Latches, • Storage Element: Flip-Flops, • Analysis of Clocked Sequential Circuits, • State Reduction and Assignment, • Design Procedure. • Synchronous Counter Design • Design Sequential Logic: Shift Registers.

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering the logic design module is to engage students actively in practical exercises to enhance their understanding and develop their critical thinking skills. The module will include a combination of classes, interactive tutorials, and hands-on experiments focused on sampling activities that capture students' interest. Through interactive classes, students will be introduced to the theoretical foundations of logic design, including explain digital system concept. express analog to digital conversion, use binary number system, realize conversion between various number systems, design fundamental digital systems, recognize logic gates, apply Boolean algebra, employ Karnaugh map for digital system optimization, develop

combinational logic circuits such as adder, subtractor, encoder, decoder, multiplexer and demultiplexer. And recognize types of Flip-flops, design sequential logic circuits. Analyze fundamental digital systems, calculate input - output relationship in digital systems, and recognize state diagrams and tables, analyses sequential logic circuits.

To reinforce learning and encourage active participation, interactive tutorials will be conducted. These tutorials will involve hands-on exercises where students will work with real-world design and apply different design techniques. This practical approach will help students grasp the practical implications of the theoretical concepts discussed in the classes.

In addition to tutorials, simple experiments will be introduced to provide students with opportunities to explore various sampling activities. These experiments will focus on real-life scenarios and problems related to digital design . Students will be encouraged to think critically, analyze the results, and propose solutions based on their understanding of the concepts learned.

The module will also emphasize the importance of collaboration and teamwork. Students will be encouraged to work together on projects and assignments, fostering a collaborative learning environment where they can exchange ideas and learn from each other's perspectives.

Overall, the module's delivery approach aims to actively engage students, refine their critical thinking skills, and provide them with practical experiences in digital design . By combining theoretical knowledge with hands-on activities, students will develop a deeper understanding of logic design concepts and their applications in various fields.

Student Workload (SWL)

الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	95	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	6
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	55	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	3
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation

تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	**Quizzes**	2	10% (10)	5 and 9	LO #1, #2 and #10, #11
	Assignments	2	10% (10)	4 and 10	LO #3, #4 and #6, #7

	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO #5, #8 and #10
Summative assessment	**Midterm Exam**	2hr	10% (10)	7	LO #1 - #7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction –Logic Design and its application
Week 2	Arithmetic Operations
Week 3	Logic Gates
Week 4	Simplification and Boolean Functions
Week 5	Logic Operations
Week 6	Combinational and Sequential Circuit Analysis Design
Week 7	Mid-term Exam
Week 8	Digital Circuit Design Optimization Methods
Week 9	Binary Adder and Substructor
Week 10	Multiplexer, Decoder, PLA
Week 11	Types of RAMs ,ROMs
Week 12	Programmable Logic Arrays
Week 13	Flip-Flops
Week 14	Counters
Week 15	Registers
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Digital binary representation
Week 2	Lab 2: Basic Gates Electronic WorkBench
Week 3	Lab 3: Two input SOP and Two input POS
Week 4	R-S flip-flop. J - K flip-flop, T Flip-Flop, D Flip-Flop

Week 5	Lab 5: - Implementation and verification of decoder, de-multiplexer and encoder, using logic gates.
Week 6	Lab 6: Implementation of 4x1 multiplexer, using logic gates.
Week 7	Lab 7: Implementation of 4-bit parallel adder, using 7483 IC
Week 8	Lab 8: Design, and verify the 4-bit synchronous counter.

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	• M. Morris Mano, "Computer System Architecture", 1998.	Yes
Recommended Texts	• Donald D. Givone (2002), Digital Principles and Design, Tata McGraw Hill. • Roth (2004), Fundamentals of Logic Design, 5th Edition, Thomson.	No
Websites	https://www.circuitlab.com/editor/#?id=7pq5wm&from=homepage https://circuitverse.org/simulator	

Grading Scheme
مخطط الدرجات

Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.